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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,887	11/13/2003	Ching-Tung Wang	4459-0448PUS1	6095

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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,887	WANG ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-19* is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. **Status:** Please all replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 08-29-2006 under amendments and request for reconsideration which have been placed of record in the file. Claims 1-19 are pending in this action.

Response to Amendment

2. The amendment filed 08-29-2006 does not introduces any new matter into the disclosure. The added material which is supported by the original disclosure.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (2002/0140711 A1) in view of Naito (US 2002/0126106 A1) and Poor (US 2004/0131279 A1).

Regarding Claim 1, Saito et al. teaches a driving circuit (page 4, paragraph 67, lines 13-15, paragraphs 68,69, page 3, paragraph 57, Lines 1-4, page 10, paragraph 138, Lines 8-10, page 5, paragraph 73,74) of a liquid crystal display device (page 3, paragraph 57, Lines 1-4), comprising: a timing controller (page 4, paragraphs 68,69) for generating a polarity inverting signal (page 10, paragraph 138, Lines 8-10) and at least one digital signal (page 5, paragraph

73,74); and a low color scale driving circuit for generating at least one analog signal in response to said polarity-inverting signal and said digital signal (page 3, paragraph 57, teaches LCD display, it is well known to one ordinary skill in the art image signal for LCD are analog signal; page 2, paragraphs 20-22 teaches it displays all the scale, high color, low color and all the intermediate color scales (color attributes) are processed to display images; page 5, paragraph 73,74 teaches timing controller generates digital and polarity invert signal).

However, Saito et al. fails to recite specifically at least one digital signal; and a low color scale driving circuit for generating at least one analog signal in response to said polarity-inverting signal and said digital signal.

However, Naito discloses at least one digital signal (page 2, paragraph 22, Lines 4,5); and a low color scale driving circuit (page 5, paragraphs 67,68, page 6, paragraphs 70,72,73, see page 4, paragraphs 53-56 and figure 2, also see page 2, paragraphs 20-22) for generating at least one analog signal in response to said polarity-inverting signal and said digital signal (page 2, paragraph 22, Lines 4-10, page 2,3 paragraph 23, page 9, paragraphs 113,114).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Naito teaching in teaching of Saito et al. to be able to have a flat panel display such as LCD display system yielding the brightness and contrast of an electro-optical device close to the best characteristic a display can offer by achieving various color scale including low color scale using gamma correction circuitry as color scale driving circuitry, inverting polarity of the digitally corrected color scale and generating analog signal to drive a display.

Saito et al. teaches a driving circuit (page 4, paragraph 67, lines 13-15).

Saito et al. fails to recite specifically low color scale.

However, Poor recite specifically low color scale (page 17, paragraph 30).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Poor teaching in teaching of Saito et al. to be able to normalizing color scale for a display by detecting highest and lowest scale color values and determining normalization parameters from detected highest and lowest scale color values and applying them.

Regarding Claim 2, Naito teaches the low color scale driving circuit (page 5, paragraphs 67,68, page 6, paragraphs 70,72,73, fig.1, item 220) further comprising: at least one buffer, receiving the polarity-inverting signal (page 4, paragraphs 52,53) and said digital signal generated from the timing controller (pages 2,3 paragraphs 22,23; page 7, paragraphs 91-94) and at least one set of transistors, coupled to an output terminal of the buffer for outputting said analog signal (page 8, paragraph 99).

Saito et al. teaches a timing controller (page 4, paragraphs 68,69) for generating a polarity inverting signal (page 10, paragraph 138, Lines 8-10).

Regarding Claim 3, Naito teaches a driving circuit of a liquid crystal display device (page 4, paragraph 57, Lines 1-4, paragraph 52, Lines1-10, pages 2,3 paragraphs 22,23; page 7, paragraphs 91-94, page 5, paragraphs 67,68, page 6, paragraphs 70,72,73, fig.1, item 220, page 8, paragraph 99) comprising a timing controller outputting a polarity-inverting signal (pages 2,3 paragraphs 22,23; page 7, paragraphs 91-94) and at least one digital signal, a source driver (page 4, paragraph 52, Lines1-10) and a low color scale driving circuit (page 5, paragraphs 67,68, page 6, paragraphs 70,72,73, fig.1, item 220, see page 4, paragraphs 53-56 and figure 2, also see page

2, paragraphs 20-22), wherein the low color scale driving circuit (page 5, paragraphs 67,68, page 6, paragraphs 70,72,73, fig.1, item 220), generating at least one analog signal (page 4, paragraph 53, Lines 1-12) comprises : at least one buffer, receiving the polarity-inverting signal (page 4, paragraphs 52,53) and said digital signal outputted from the timing controller (pages 2,3 paragraphs 22,23; page 7, paragraphs 91-94); and at least one set of transistors, coupled to an output terminal of the buffer for outputting said analog signal (page 8, paragraph 99, see page 4, paragraphs 53-56 and figure 2, also see page 2, paragraphs 20-22).

Saito et al. teaches a timing controller (page 4, paragraphs 68,69) for generating a polarity inverting signal (page 10, paragraph 138, Lines 8-10).

Allowable Subject Matter

5. Claims 5-19 are allowed.

6. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance:

A driving circuit of a liquid crystal display device including a timing controller, a source driver and a low color scale driving circuit, **the timing controller outputting a polarity-inverting signal, a first digital signal, a second digital signal, a third digital signal and a**

fourth digital signal, the low color scale driving circuit generating a first analog signal, a second analog signal, a third analog signal and a fourth analog signal and comprising: a plurality of buffers, receiving the polarity-inverting signal, the first digital signal, the second digital signal, the third digital signal and the fourth digital signal; and a plurality of sets of transistors which comprise a first set of transistors, a second set of transistors, a third set of transistors, and a forth set of transistors, respectively coupled to an output terminal of the buffers for respectively outputting the first, second, third and fourth analog signal .

Cited references on 892's fail to recite or disclose above bold underlined claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

8. Applicant's arguments filed 08-29-2006 have been fully considered but they are not persuasive.

Applicant argues the cited combination of Saito et al. (2002/0140711 A1) in view of Naito (US 2002/0126106 A1) and Poor (US 2004/0131279 A1) fail recite or disclose claimed limitations; specifically low scale color driving circuitry.

Examiner disagrees Saito et al. teaches at least one digital signal (page 5, paragraph 73,74); and a low color scale driving circuit for generating at least one analog signal in response to said polarity-inverting signal and said digital signal (page 3, paragraph 57, teaches LCD display, it is well known to one ordinary skill in the art image signal for LCD are analog signal; page 2, paragraphs 20-22 teaches it displays all the scale (attributes), high color, low color and all the intermediate color scales are processed to display images; page 5, paragraph 73,74 teaches timing controller generates digital and polarity invert signal).

Naito does teach color scale driving circuitry has 10 (ten) bits color data which will produce 1024 gray scales, which does include lower scale color data to higher gray scale color data (page 5, paragraph 65, page 7, paragraphs 86-90) and this are digital signal and further after gamma correction it converts into analog signal via D/A and polarity inversion circuit performs polarity inversion in transmitted in parallel to D/A converting digital signal into analog signal and analog polarity inverting circuit reverses the polarity of the analog picture signal in an analog form in the specified cycle (see page 4, paragraphs 53-56 and figure 2, also see page 2, paragraphs 20-22). It is also well known to one ordinary skill in the art that low scale colors are text messages or alphanumeric entries. When image processors are processing all the gray scales; not only it is processing text messages, it also processes high resolution images (see Tjandra et al. US 2003/0034942 A1 filing date August 16, 2001, page 3, paragraphs 37-39); and Poor recite specifically low color scale (page 17, paragraph 30). Combination teaches applicant's claimed limitations; therefore they do obviate.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

11. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

AU2629

October 11, 2006

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